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**DECLARATION OF NORIKO KOMORIYA**

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Sir:

Noriko Komoriya declares under penalty of perjury under the laws of the United States of America as follows:

1. I am a citizen of Japan currently employed at Suto International Patent Office in Ota-shi, Gunma-ken, Japan. I have a good command both in English and Japanese languages.

2. I have translated Japanese Patent Application No. 2002-326413, and the translation is a literal translation of the Japanese patent application.

I declare under penalty of perjury under the laws of the United Stares that the foregoing is true and correct. Executed at Ota-shi, Gunma-ken, Japan, this 6th day of December, 2005.

Noriko Komoriya

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[Title of the Invention] Display Device

[Claims]

[Claim 1] A display device comprising:

a plurality of pixels disposed in a matrix configuration;

a plurality of gate lines extending in a row direction; and

a vertical driving circuit supplying a gate scanning signal to a plurality of the gate lines, each of the pixels selected according to the gate scanning signal;

wherein the gate line is severed before the gate line reaches an output portion of the vertical driving circuit from the pixel and the separated gate lines are connected by a metal wiring in an upper layer.

[Claim 2] The display device of claim 1, wherein the distance between the separated gate lines is larger than 10μm.

[Claim 3] The display device of claim 1, wherein the distance between the edge of the separated gate line and a gate wiring in the output portion of the vertical driving circuit is larger than 10μm.

[Claim 4] The display device of claim 1, wherein the device has the two gate lines, the gate line of the pixel and the gate line located close to the output portion of the vertical driving circuit, before the separated gate lines are connected by the metal wiring in an upper layer.

[Claim 5] The display device of claim 1, wherein the gate line comprises either molybdenum layer or chrome layer.

[Claim 6] The display device of claim 1, wherein the metal wiring comprises aluminum layer.

[Claim 7] A display device comprising:

a plurality of pixels disposed in a matrix configuration;

a plurality of gate lines extending in a row direction;

a plurality of data lines extending in a column direction;

a vertical driving circuit supplying a gate scanning signal to a plurality of the gate lines; and

a horizontal driving circuit generating a drain scanning signal for controlling the timing of supplying a video signal to a plurality of the data lines;

wherein a gate wiring in a thin film transistor configuring a circuit in the vertical driving circuit or the horizontal driving circuit is severed and the separated gate wirings are connected by a metal wiring in an upper layer.

[Claim 8] A display device comprising:

a plurality of pixels disposed in a matrix configuration;

a plurality of gate lines extending in a row direction;

a plurality of data lines extending in a column direction;

a vertical driving circuit supplying a gate scanning signal to a plurality of the gate lines; and

a horizontal driving circuit generating a drain scanning signal for controlling the timing of supplying a video signal to a plurality of the data lines;

wherein the gate wiring is severed in such a way that the single gate wiring is not directly inputted to a plurality of the thin film transistors in either the vertical driving circuit or the horizontal driving circuit and the separated gate lines are connected by a metal wiring in an upper layer.

[Claim 9] The display device of claim 8, wherein a gate wiring other than the gate wiring is inputted to at least one of the thin film transistors among a plurality of the said thin film transistors.

[Claim 10] The display device of claim 8 or 9, wherein a plurality of the thin film transistors means more than three thin film transistors.

[Claim 11] A display device comprising:

a plurality of pixels disposed in a matrix configuration;

a plurality of gate lines extending in a row direction;

a plurality of data lines extending in a column direction;

a vertical driving circuit supplying a gate scanning signal to a plurality of the gate lines; and

a horizontal driving circuit generating a drain scanning signal for controlling the timing of supplying a video signal to a plurality of the data lines;

wherein the gate wiring is severed in such a way that the single gate line is not directly inputted to a plurality of active layers in either the vertical driving circuit or the horizontal driving circuit and the separated gate wirings are connected by a metal wiring in an upper layer.

[Claim 12] The display device of claim 11, wherein a gate wiring other than the said gate wiring is inputted to at least one of the active layers among a plurality of the said active layers.

[Claim 13] The display device of claim 11 or 12, wherein a plurality of the active layers means more than three active layers.

[Claim 14] A display device comprising:

a plurality of pixels disposed in a matrix configuration;

a plurality of gate lines extending in a row direction;

a plurality of data lines extending in a column direction;

a vertical driving circuit supplying a gate scanning signal to a plurality of the gate lines; and

a horizontal driving circuit generating a drain scanning signal for controlling the timing of supplying a video signal to a plurality of the data lines;

wherein an active layer is severed in such a way that a plurality of gate lines, not being the same signal line, is not inputted to the single active layer in either the vertical driving circuit or the horizontal driving circuit and the separated active layers are connected by a metal wiring in the layer upper than the layer of the gate wiring.

[Claim 15] A display device comprising:

a plurality of pixels disposed in a matrix configuration;

a plurality of gate lines extending in a row direction;

a plurality of data lines extending in a column direction;

a vertical driving circuit supplying a gate scanning signal to a plurality of the gate lines; and

a horizontal driving circuit generating a drain scanning signal for controlling the timing of supplying a video signal to a plurality of the data lines;

wherein an active layer is severed in such a way that three or more gate lines, not being the same signal line, are not inputted to the single active layer in either the vertical driving circuit or the horizontal driving circuit and the separated active layers are connected by a metal wiring in the layer upper than the layer of the gate wiring.

[Claim 16] The display device of claim 14 or 15, wherein the active layer forms a multiple gate type thin film transistor.

[Claim 17] A display device comprising:

a plurality of pixels disposed in a matrix configuration;

a plurality of gate lines extending in a row direction;

a plurality of data lines extending in a column direction;

a vertical driving circuit supplying a gate scanning signal to a plurality of the gate lines; and

a horizontal driving circuit generating a drain scanning signal for controlling the timing of supplying a video signal to a plurality of the data lines;

wherein only one gate wiring is inputted to the one active layer in either the vertical driving circuit or the horizontal driving circuit

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

This invention relates to a display device that has a plurality of pixels disposed in a matrix configuration, a plurality of gate lines extending in a row direction, and a vertical driving circuit sequentially supplying a gate scanning signal to each of the gate lines, especially to a method for preventing electro-static break down.

[0002]

[Background Art]

Fig. 10 is a diagram of the conventional liquid crystal display device. A liquid crystal panel 100 has a plurality of pixels formed in a matrix configuration of n-rows and m-columns. Each of the pixels has a pixel selecting thin film transistor TFT 10, a liquid crystal LC, and a storage capacitor Csc. The thin film transistor will be referred to as TFT hereinafter.

[000 3]

A gate line 20 extending in a row direction is connected to the gate of the TFT 10, and a data line 22 extending in a column direction is connected to the drain of the TFT 10. A gate scanning signal is sequentially supplied from a vertical driving circuit (V drive circuit) 130 to the gate line 20 of each row and the TFT 10 is selected accordingly. Also, a video signal is applied to the liquid crystal LC through the TFT 10 based on a drain scanning signal supplied from a horizontal driving circuit (H drive circuit) 140. (See Patent Document 1, for example.)

[000 4]

[Patent Document 1]

Japanese Patent Application Publication No. Hei 10-115839.

[0005]

[Problem to be solved by the Invention]

However, a gate insulating layer of the TFT in the output portion of the gate scanning signal of the vertical driving circuit 130, sometimes suffers from the break down and the leakage due to static electricity during the TFT manufacturing process of the conventional liquid crystal display device. This kind of trouble will be addressed by referring to Fig. 8. Fig. 11 is enlarged figures of the part B enclosed with the dotted line in Fig. 10. These figures show the pattern of the edge of the gate line 20 as well as the output portion of the vertical driving circuit 130. Fig. 11(A) is a plan view and Fig. 11(B) is a cross-sectional view along with the X-X line in Fig. 11(A).

[000 6]

Dry-etching method is employed for processing the gate line 20, a storage capacitor line 21, and a gate wiring in the vertical driving circuit 130. Static electricity is stored in the gate line 20, the storage capacitor line 21, and the gate wiring during the dry-etching process. When the ion implantation of an N-type impurity such as arsenic or phosphorus into a P-Si layer (the ion implantation of a P-type impurity such as boron in case of P-type channel TFT) is performed for forming a source region and a drain region using the gate line 20 as a mask, static electricity is also stored in the gate line 20, the storage capacitor line 21, and the gate wiring due to the charge-up phenomena. It is especially easy for the gate line 20 and the storage capacitor line 21 to store static electricity because they extend across the liquid crystal panel 100.

[000 7]

The stored electricity is discharged from the edge of the gate line 20 to the gate wiring 13 of the TFT 1 located close to the gate line 20, as shown in Fig. 11. The charges from the discharge will reach a gate electrode of an adjacent TFT 2 through the gate wiring 13, causing the dielectric break down and the leakage of the part A of the gate insulating layer 12 of the TFT 2-1. In the figure, the reference numeral 40 indicates a transparent insulating substrate, the reference numeral 11 denotes an active layer (poly-silicon layer)

disposed on the transparent insulating substrate 40, and the reference numeral 14 indicates an aluminum wiring layer. Fig. 11(B) is a cross-sectional view of the device before the aluminum wiring layer 14 is disposed.

[0008]

[Means for solving the Problems]

This invention is to offer the countermeasure against the break down of the device due to static electricity that takes place during the manufacturing process of the liquid crystal display device.

[000 9]

First, in this invention, a gate line 20 is severed before it reaches the output portion of a vertical driving circuit 130, as shown in Figs. 1 and 2. The separated gate lines 20 and 20 are connected by a metal wiring 25 located in an upper layer.

[00 10]

Second, a gate wiring line 153 of a TFT, a portion of the vertical driving circuit 130, is severed as shown in Fig. 4. The separated gate wiring lines 153 and 153 are connected by a metal wiring 153A located in an upper layer.

[00 11]

Third, the gate wiring line in the vertical driving circuit 130 is severed as shown in Fig. 4, so that the gate wiring line will not make a direct input into more than three thin film transistors. The separated gate wiring lines 153 and 153 are connected by the metal wiring 153A located in an upper layer.

[00 12]

Fourth, an active layer is severed as shown in Fig. 6(B) and Fig. 6(C), so that no more than two gate wirings extends above the single active layer in case of a multi-gate type TFT, where more than three different kinds of signals in the vertical driving circuit 130 is inputted through the gate wiring. The separated active layers are connected by a metal wiring located in a layer above the gate wiring.

[0013]

[Description of the Invention]

A detailed description about this invention will be made by referring to figures.

( The First Embodiment)

Fig. 1 is a diagram of the liquid crystal display device of the first embodiment of this invention. The same components as those shown in Fig. 7 have the same reference numerals and the explanation on those components will be omitted. In this liquid crystal display device, a gate line 20 is severed before the gate line 20 reaches the output portion of a vertical driving circuit 130 and the separated gate lines 20 and 20 are connected by a metal wiring 25 located in an upper layer (see the part C enclosed by the dotted line in Fig. 1).

The gate line 20 is made of, for example, molybdenum (Mo) or chrome (Cr), and the metal wiring 25 is made of aluminum.

[00 14]

Fig. 2 is enlarge figures of the part C enclosed by the dotted line in Fig. 1. These figures show the patterns of the edge of the gate line 20 and the output portion of the vertical driving circuit 130. Fig. 2(A) is a plan view, and Fig. 2(B) is a cross-sectional view along with the X-X line in Fig. 2(A).

[00 15]

Since the gate line 20 is severed, the voltage stored in the gate line 20 during the manufacturing process of the liquid crystal display device will not be directly discharged to a gate wiring 13 of a TFT 1. Therefore, the break down of a gate insulating layer 12 of the TFT is prevented.

[00 16]

The separated gate lines 20 and 20 are both connected to the metal wiring 25 located above the gate lines 20, 20 through contact holes formed in an interlayer insulating layer (not shown in the figure).

[00 17]

It is preferable to have an interval of more than 10μm between the separated gate lines 20, 20. According to the inventor, the probability for the discharge to take place between the wirings in the same layer gets smaller when the interval between the wirings gets bigger. When the interval between the wirings is more than 10μm, the probability of

the electric discharge can be minimized.

[00 18]

If the edge of the gate line is located close to a pixel portion before it is severed from the TFT 1 in the output portion of the vertical driving circuit, the discharge from the gate line 20 of the pixel portion side may be directed toward the gate wiring of the TFT 1, not toward the separated gate line 20, as seen from Fig. 2. Therefore, the location where the gate line 20 is severed ought to be apart at least 10μm from the TFT 1 of the output portion of the vertical driving circuit for preventing the discharge described above.

[00 19]

With this configuration, the discharge from the gate line 20 will never directly go to the gate wiring of the TFT 1. The discharge may go to the gate line 20 first, and then be directed toward the gate wiring of the TFT 1.

[00 20]

According to the inventor of this invention, the amount of charges stored in the long wiring such as the gate line is usually large. If this large amount of charges is directly discharged to the gate wiring of TFT, the gate insulating layer may be broken down or damaged, causing the leakage of the electric current. However, the charges stored in the gate line will be much smaller in amount when the gate line is severed, making the shorter gate line.

[00 21]

Thus, even if the charges stored in the shorter gate line are discharged to the gate wiring of the TFT, the damage to the insulating layer of the TFT will be much smaller and the possibility to cause the deterioration of the TFT will also be reduced.

[00 22]

Therefore, the severance of the gate line, the separation of the gate line from the gate wiring of the TFT in the output portion, and the using of the shorter gate line between the original gate line and the output portion are the effective countermeasures against the electro-static damage.

[00 23]

The manufacturing processes explained above are from the process of forming the gate wiring to the previous process of the forming of the metal wiring. Those processes are especially vulnerable against the electro-static damage because entire surface except the gate wiring portion is covered with the insulating layer. Therefore, as a countermeasure against the electro-static damage, it is effective to separate the gate wiring during these processes and to connect the gate wirings by the metal wiring afterwards.

[00 24]

(The Second Embodiment)

This embodiment is to prevent the electro-static break down of the gate insulating layer within the vertical driving circuit 130 and a horizontal driving circuit 140. Here, the preventive measures of the electro-static break down will be explained by using the vertical driving circuit 130 as an example. The same measures can be equally effective for the horizontal driving circuit 140.

[00 25]

Fig. 3 is a diagram of the vertical driving circuit 130. The vertical driving circuit 130 has a shift register 131, a two-directional scanning portion, and an output portion 133 that outputs a gate scanning signal to the gate line 20. The two-directional scanning portion 132 has a plurality of three- input NAND gates 134A, 134B, 134C and 134D.

[00 26]

A clock signal of a clock signal line 151 is commonly inputted to each of the three-input NAND gates. The gate wiring 153 from the shift register 131 is inputted to both the input NAND gates 134A and 134B. A gate wiring 154 from the shift register 131 is inputted to both the input NAND gates 134B and 134C. And a gate wiring 155 from the shift register 131 is inputted to both the input NAND gates 134C and 134D.

[00 27]

Fig. 4 shows the pattern of the portion enclosed with the dotted line in Fig. 3. The characteristic of this pattern is that the gate wiring 153 commonly inputted to TFTs 161, 162, which configures the three-input NAND gate 134A, and TFTs 163, 164, which configures the input NAND gate 134B adjacent to the three- input NAND gate 134A, is severed. And the

separated gate wirings 153 and 153 are connected by a metal wiring 153A in an upper layer.

[00 28]

Likewise, the gate wiring 154 is severed and the separated gate wirings 154 and 154 are connected by a metal wiring 154A in an upper layer. The gate wirings 153 and 154 are made of, for example, molybdenum (Mo) or chrome (Cr) and the metal wiring 153A and 154A are made of aluminum.

[00 29]

The mechanism of electro-static break down of the gate insulating layer of the TFT, where the gate wirings 153, 154 are not separated, will be explained below.

[00 30]

When static electricity is discharged from a gate wiring 171 to a gate wiring 152-1, the closest wiring to the gate wiring 171, the break down of the gate insulating layer between a poly-silicon layer (active layer) of the TFT 161 and the gate wiring 152-1 is likely to take place. When the electric potential of the poly-silicon layer of the TFT 161 changes suddenly due to the break down, the electrical potential of the gate wirings 151 and 153-1, which make capacitance coupling with the poly-silicon layer of the TFT 161, also changes drastically. Since the gate wiring 153 is inputted to the TFT 163, there will be a big discrepancy in voltage between the poly-silicon layer of the TFT 163 and the gate wiring 153, damaging a gate oxide film.

[00 31]

When the gate wirings 153 and 154 are not separated, electro-static break down or damage will be transmitted to the adjacent poly-silicon island due to the capacitance coupling between the poly-silicon and the gate. However, it is possible to lower the amount of charges stored in one gate line and to prevent the transmission of the electro-static break down from one poly-silicon island to another poly-silicon island. The gate wirings will be connected by the metal wiring at the final stage. However, it is effective to separate the gate wirings during the processes vulnerable against the electro-static break down.

[00 32]

Electro-static damage is transmitted when at least one of the poly-silicon islands,

among a plurality of the poly-silicon islands (the gate wiring 153 is inputted into four poly-silicon islands), to which a single gate line is inputted, is provided with the gate signal from another gate line. In other words, when there are a plurality of poly-silicon islands with the single gate wiring inputted, and when at last one of these poly-silicon islands has another gate wiring inputted, the gate wiring should be separated. Then, the separated gate wirings should be connected by the metal wiring in an upper layer in the later process.

[00 33]

Each of three input signals is inputted to the poly-silicon island of P-channel side and the poly-silicon island of N-channel side in the three- input NAND circuit shown in Fig. 4. Each of the gate wirings 152, 153, and 154, is inputted to the two poly-silicon islands, and the gate wiring 151 is inputted to each of the poly-silicon islands as an independent wiring respectively. In terms of the prevention of the electro-static damage, the gate wiring 151 is preferable.

[00 34]

The gate wiring 13 shown in Fig. 11 is also inputted to the two poly-silicon islands shown as the TFT 1 and TFT 2-1. When the gate wiring is severed as shown in Fig. 7, the possibility for the static electricity discharged from the gate line 20 to damage the TFT 2 will be reduced.

[00 35]

The circuit in the vertical driving circuit 130 has been used as an example in the above explanation, but it is also true that the charges are stored in a long gate wiring during the manufacturing process in the horizontal driving circuit 140. The same countermeasure against the electro-static damage can be taken for the horizontal driving circuit 140.

[00 36]

According to the inventor of this invention, a large amount of charges is stored during the manufacturing process of the liquid crystal display device (the dry-etching process of the gate wiring, and the ion implantation process for forming the source and drain region at a later stage) due to the charge-up mechanism when the device has a long gate wiring. Therefore, the gate insulating layer of the thin film transistor is likely to be damaged due to

the discharge of the electricity. Thus, the gate wiring should be severed for reducing the voltage stored.

[00 37]

Fig. 5 is cross-sectional views that show the concept of this invention. A gate insulating layer 203 is likely to be damaged by the static electricity when the long gate wirings 201 extends over the poly-silicon islands 200-1, 200-2, --- of the thin transistor with the gate insulating layer 203 between them, as shown in Fig. 5(A).

[00 38]

Therefore, the gate wirings 201-1, 201-2, --- are severed as shown in Fig. 5(B), and the separated gate wirings are connected by an aluminum wiring in an upper layer in the later manufacturing process.

[00 39]

Also, the gate wirings 153, 154 are severed, as seen from Fig. 4, so that they would not be directly inputted to more than three TFTs. For example, the gate wiring 153 is severed and one of the separated gate wiring is inputted to the thin film transistors 161, 162 of the three- input NAND circuit 134A and another separated gate wiring is inputted to the thin film transistors 163, 164 of the three- input NAND circuit 134B respectively.

[00 40]

In this case, the gate wiring 153 is inputted directly only to two TFTs. This is the preferable configuration because the gate insulating layer of the TFT is likely to be damaged, if a single gate wiring is directly inputted to many of the TFTs. The gate wiring should not be inputted directly to more than three TFTs. However, it is not practical if the number of the TFT, to which the same gate wiring is inputted directly, is limited to less than two.

[00 41]

(The Third Embodiment)

The first and second embodiments explained above are about the prevention of the electro-static damage taken in the gate wiring. The third embodiment is about the prevention of the electro-static damage taken in terms of the poly-silicon island (the poly-silicon active layer) of the TFT. The poly-silicon active layer is severed in such a way

that a plurality of the different gate wirings will not be inputted to a single poly-silicon island in the driving circuit (both the vertical driving circuit and the horizontal driving circuit). Then, the separated poly-silicon islands are connected later by the metal wiring located in a layer upper than the layer of the gate wiring.

[00 42]

The poly-silicon island in Fig. 11 is configured from the TFT 2-1 with the gate wiring 13 inputted and the TFTs 2-2, 2-3 with the gate wiring 15 inputted.

[00 43]

When the electric discharge due to static electricity is inputted to the gate wiring 13, making a big change in the voltage of the gate wiring 13, the difference in the voltage between the gate wiring 15 and the gate wiring 13 becomes large. Since the poly-silicon film makes capacitance couplings with both of the gate wirings, there should be a big difference in the voltage in the insulating layer, causing the break down of the insulating layer.

[00 44]

In order to prevent the problem described above, the poly-silicon islands are separated, as shown in Fig. 8. Each poly-silicon island is provided with one of the gate wirings. The change in the voltage of the gate wirings due to static electricity will only influence the poly-silicon island to which each of the gate wirings is inputted. The poly-silicon island makes a capacitance coupling only with the gate wiring that is inputted to this particular poly-silicon island. Therefore, the break down of the insulating layer is less likely to take place.

[00 45]

The separated poly-silicon islands work in the same way as the circuit shown in Fig. 8 when they are connected by the metal wiring. The configuration, where a plurality of the gate wirings are not inputted to a single poly-silicon island, is also effective when the poly-silicon island configures a multi gate transistor.

[00 46]

Fig. 6 shows the pattern examples (A), (B), and (C) of the three- input gate type TFT.

For example, this corresponds to the N-type TFT of the three-input NAND circuit (see the TFTs 161, 163 in Fig.4).

[00 47]

The drawings in left side are the plan views of the pattern, and the drawings in right side shows the cross-sectional views along with the X-X line, Y-Y line and Z-Z line of the plan views respectively. Three different signals C1, C2, and C3 are inputted to each of the gate wirings in each pattern.

[00 48]

In the pattern example of (A), the three gate wirings are inputted above a single poly-silicon island 300. The dielectric break down and the leakage of the gate insulating layer 400 is very likely to take place in this pattern.

[00 49]

In this pattern, there would be a big voltage difference between any two of the three gate wirings during the process when static electricity is stored and discharged, causing the dielectric break down. Therefore, this pattern is avoided, by the design rule, in this embodiment. Rather the pattern examples (B) and (C) are employed.

[00 50]

The poly-silicon islands of the three-input TFT are divided into two poly-silicon islands 301 and 302 in the example of (B). Two gate wirings extend over the poly-silicon island 301 with the insulating layer 400 between them and one gate wiring extends over the other poly-silicon island 302 adjacent to the poly-silicon island 301.

[00 51]

Two poly-silicon islands 301 and 302 are connected by the metal wiring 303 in an upper layer during the later manufacturing process, functioning as a single three-way input TFT.

[00 52]

The poly-silicon islands of the three-input TFT are divided into three poly-silicon islands 304, 305, and 306 in the example of (C). One gate wiring extends over each of the poly-silicon islands with the insulating layer 400 between them.

[00 53]

The three poly-silicon islands 304, 305 and 306 are connected by metal wirings 307 and 308 in an upper layer during the later manufacturing process, functioning as a single three-way input thin film transistor.

[00 54]

The explanation has been made on each of the above embodiments by using the liquid crystal display device as an example. However, this invention is not limited to this application. It can be broadly applied to the device with a gate line and a vertical driving circuit, such as an organic EL display device.

[00 55]

It is preferable to divide the poly-silicon islands of the three-input NAND N-channel type TFT into three, rather than two.

[00 56]

Also, when the separation of the gate wiring shown in Fig. 7 and the separation of the poly-silicon island shown in Fig. 8 are combined, we have the configuration where one gate wiring is inputted to a single poly-silicon island as shown in Fig. 9.

[00 57]

[Effect of the Invention]

According to this invention, the gate line is severed before the gate line reaches the output portion of the vertical driving circuit, and the separated gate lines are connected by the metal wiring in an upper layer. Therefore, influence from static electricity during the manufacturing process can be eliminated, preventing the dielectric break down and the dielectric leakage of the output portion of the TFT.

[00 58]

Additionally, the gate wiring of the TFT configuring the vertical driving circuit or the horizontal driving circuit is severed, and the separated gate wirings are connected by the metal wiring in an upper layer. Therefore, the amount of static electricity stored in the gate wiring can be reduced, preventing the dielectric break down and the dielectric leakage of the TFT.

[00 59]

Also, the gate wiring in the vertical driving circuit is severed in such a way that no single gate wiring is inputted to a plurality of the TFTs or the active layers. The separated gate wirings are connected by the metal wiring in an upper layer. Therefore, the dielectric break down and the dielectric leakage of the TFT can be prevented.

[00 60]

The active layer, where a plurality of the gate wirings are inputted, is severed in such a way that no more than two gate wirings extends in the same single active layer, and the separated active layers are connected by the metal wiring in an upper layer. Therefore, the dielectric break down and the dielectric leakage of the multi-gate type TFT can be prevented.

[Brief Description of the Drawings]

[Fig. 1]

Fig. 1 is a diagram of the liquid crystal display device of the embodiment of this invention.

[Fig. 2]

Fig. 2 is diagrams of the output portion of the vertical driving circuit of the liquid crystal display device of the embodiment of this invention.

[Fig. 3]

Fig. 3 is a diagram of the vertical driving circuit of the liquid crystal display device of the embodiment of this invention.

[Fig. 4]

Fig. 4 shows a partial pattern of the vertical driving circuit of the liquid crystal display device of the embodiment of this invention.

[Fig. 5]

Fig. 5 is partial cross-sectional views of the vertical driving circuit of the liquid crystal display device of the embodiment of this invention.

[Fig. 6]

Fig. 6 shows examples of the pattern (A), (B), and (C) of the input-gate-type thin film transistor.

[Fig. 7]

Fig. 7 is diagrams of the output portion of the vertical driving circuit of the liquid crystal display device of the embodiment of this invention.

[Fig. 8]

Fig. 8 is a diagram of the output portion of the vertical driving circuit of the liquid crystal display device of the embodiment of this invention.

[Fig. 9]

Fig. 9 is a diagram of the output portion of the vertical driving circuit of the liquid crystal display device of the embodiment of this invention.

[Fig. 10]

Fig. 10 is a diagram of the conventional liquid crystal display device.

[Fig. 11]

Fig. 11 is diagrams of the output portion of the vertical driving circuit of the conventional liquid crystal display device.

[Description of Numerals]

11 active layer

12 gate insulating layer

13 gate wiring

14 metal wiring

20 gate line

21 storage capacitor line

22 data line

25 metal wiring

40 transparent insulating substrate

100 liquid crystal panel

130 vertical driving circuit

| | |
|---|---|
| 131 | shift register |
| 132 | two-directional scanning portion |
| 133 | output portion |
| 134A-134D | NAND gate |
| 140 | horizontal driving circuit |
| 153-156 | gate wiring line |
| 161-164 | thin film transistor |
| 200 | poly-silicon island |
| 201 | gate wirings |
| 203 | gate insulating layer |

[Document Name] Abstract

[Summary]

[Subject] The invention prevents dielectric break down and dielectric leakage of a gate insulating layer of a thin film transistor in a display device.

[Solving Means] The gate line 20 is severed before the gate line 20 reaches the output portion of the vertical driving circuit 130, and the separated gate lines 20, 20 are connected by the metal wiring 25 in an upper layer. The gate line 20 is, for example, made of molybdenum (Mo) or chrome (Cr) and the metal wiring 25 is made of aluminum since the gate line 20 is severed, the voltage stored in the gate line 20 during the manufacturing process will not be discharged to the gate wiring 13 of the thin film transistor 1, preventing the break down of the gate insulating layer 12 of the thin film transistor TFT 12.

[Selected Figure] Fig. 2